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EXAMINER	
RUTZ, JARED IAN	
ART UNIT	**PAPER NUMBER**
2187	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/802,010	CHUNG ET AL.	
	Examiner	Art Unit	
	Jared I. Rutz	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-15 and 17* is/are rejected.

7)☒ Claim(s) *7 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-17, as amended on 11/27/2006, are pending in the instant application. Applicant's arguments filed 11/27/2006 have been carefully and fully considered, but are only found partially persuasive as discussed infra. Accordingly, this Office action is made **FINAL**.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. **Claims 2 and 12** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

4. **Claims 2 and 12** recite the limitation "*The method as claimed in claim 11, wherein the meta-information is written after the data of the logical block is written.*". The Examiner is not aware of a portion of the specification which teaches how the meta-information is written after the data of the logical block is written. Accordingly, one of

ordinary skill in the art would not know how to make or use the invention as recited in claims 2 and 12.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. **Claims 1, 3-4, 11, and 13-14** are rejected under 35 U.S.C. 102(b) as being anticipated by Conley (US 2002/0099904).

7. **Claim 1** is taught by Conley as:

a. *A flash memory access apparatus, comprising: a flash memory comprising a plurality of units, each of the units comprising a plurality of blocks, and a flash memory controller.* Paragraph 0038 teaches the architecture of a typical non-volatile data storage system, which includes a controller and a plurality of flash memory devices. Paragraph 0040 explains that flash memory cells are divided into multiple pages.

b. *Wherein if a write operation is requested for a logical block number of the flash memory, the flash memory controller is configured to write data and meta-information in a physical block corresponding to a logical block with the logical block number if a previous write operation has not been performed for the logical*

block. Paragraph 0062 discusses a method of programming a non-volatile memory. If there are pages in the physical block that have not been written to, the data is written to those blocks.

c. *And the flash memory controller is configured to perform a write operation for writing the data and the meta-information allocated to the logical block in a new physical block without changing flash memory state information written in a previous physical block corresponding to the logical block if the previous write operation has been performed for the logical block*. Paragraph 0049 shows that when new data is to be written to a logical block corresponding to physical block PBN 0, item 35 of figure 8, which is full, a new physical block PBN 1, item 39 of figure 8, is selected and the new pages are written to PBN 1. Paragraph 0055 shows that an individual page contains data, item 45 of figure 10, and meta-information, item 49 of figure 10. Paragraph 0048 shows that when new pages are written to a logical block, the pages containing the original data are not tagged. The last sentence of paragraph 0047 further emphasizes this by stating "*the writing of the old/new or other flags, as described with respect to FIGS. 6, 7A and 7B, cannot be tolerated.*"

8. **Claim 3** is taught by Conley as:

d. *The apparatus as claimed in claim 1, wherein the data and meta-information of the logical block are simultaneously written*. Paragraph 0055 shows that the data 45 and meta-information 49 are part of the same page. As

the data and meta-information are part of the same page they would inherently be written simultaneously, as the system of Conley writes data on a page basis.

9. **Claim 4** is taught by Conley as:

e. *The apparatus as claimed in claim 1, wherein the meta-information comprises the logical block number.* Paragraph 0055 shows that overhead data, item 49 of figure 10, contains the logical block number.

f. *And the flash memory state information indicating a state of the physical block as valid, deleted, or invalid.* Paragraph 0055 shows a page contains a time stamp. Paragraph 0050 shows that the time stamp indicates the time the page was written relative to other pages with the same logical address. As shown in paragraph 0052, the time stamps of blocks having the same logical block address and page offset are compared, which allows the system to determine which page is the last written page. Accordingly, this shows what pages are valid.

10. **Claim 11** is taught by Conley as:

g. *A flash memory access method, comprising: accessing the flash memory and searching for a currently writable physical block if a processor requests a write operation for a specific logical block number of the flash memory.* Paragraph 0062 shows that when a write is performed, an available physical page is found.

h. *And writing data and meta-information in a physical block corresponding to a logical block with the logical block number if a previous write operation has not been performed for the logical block.* Paragraph 0062 discusses a method of programming a non-volatile memory. If there are pages in the physical block that have not been written to, the data is written to those blocks.

i. *And writing the data and the meta-information in a new physical block corresponding to the logical block without changing flash memory state information written in a previous physical block corresponding to the logical block the previous write operation has been performed for the logical block.* Paragraph 0049 shows that when new data is to be written to a logical block corresponding to physical block PBN 0, item 35 of figure 8, which is full, a new physical block PBN 1, item 39 of figure 8, is selected and the new pages are written to PBN 1. Paragraph 0055 shows that an individual page contains data, item 45 of figure 10, and meta-information, item 49 of figure 10. Paragraph 0048 shows that when new pages are written to a logical block, the pages containing the original data are not tagged. The last sentence of paragraph 0047 further emphasizes this by stating "*the writing of the old/new or other flags, as described with respect to FIGS. 6, 7A and 7B, cannot be tolerated.*"

11. **Claim 13** is taught by Conley as:

j. *The apparatus as claimed in claim 11, wherein the data and meta-information of the logical block are simultaneously written.* Paragraph 0055

shows that the data 45 and meta-information 49 are part of the same page. As the data and meta-information are part of the same page they would inherently be written simultaneously, as the system of Conley writes data on a page basis.

12. **Claim 14** is taught by Conley as:

k. *The method as claimed in claim 11, wherein the meta-information comprises the logical block number.* Paragraph 0055 shows that overhead data, item 49 of figure 10, contains the logical block number.

l. *And the flash memory state information indicating a state of the physical block as valid, deleted, or invalid.* Paragraph 0055 shows a page contains a time stamp. Paragraph 0050 shows that the time stamp indicates the time the page was written relative to other pages with the same logical address. As shown in paragraph 0052, the time stamps of blocks having the same logical block address and page offset are compared, which allows the system to determine which page is the last written page. Accordingly, this shows what pages are valid.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. **Claims 5-6, 8-10, 15, and 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Conley (cited *supra*) in view of Kim et al. (US 6,381, 176).

15. **Claim 5** is taught by Conley as shown *supra* with respect to claim 1.

16. Although Conley teaches that blocks having the same logical block number can be distinguished by their timestamps, it does not disclose expressly performing a recovery operation.

17. With respect to claim 5, Kim teaches:

m. *The apparatus as claimed in claim 1, wherein the flash memory controller is configured to perform a recovery operation which detects, during a scanning process, physical blocks for the logical block number and recovers from an error by determining a valid block for the logical block among the detected physical blocks.* Kim teaches at column 6 lines 29-36 that a recovery operation is required if two valid blocks having the same logical block number exist. In the system disclosed by Conley, paragraph 0050 shows that it can be determined which of multiple pages having the same logical block number and page offset is the correct page by comparing the timestamps of the blocks.

18. At the time of the invention it would have been obvious to one of ordinary skill in the art that a recovery operation is necessary in the event of an error during writing.

19. Conley and Kim are analogous art because they are from the same field of endeavor, the design of flash memory systems.

20. The motivation for doing so would have been to determine which block will be erased during a recovery operation (Kim, column 6 lines 30-36)

21. Therefore, it would have been obvious to combine Kim with Conley for the benefit of determining which pages are old and can be deleted to obtain the invention as specified in **claims 5, 6, and 8-10**.

22. **Claim 6** is taught by Conley as:

n. *The apparatus as claimed in claim 5, wherein the scanning process comprises reading a logical block number for each of the physical blocks by investigating the flash memory based on a latest accessed block.* Paragraph 0052 shows that when the controller reads the data, it compares the counts in fields 43 and 43' of pages having the same LBA and page offset.

o. *And investigating a field of a block allocation table corresponding to the read logical block number.* Figure 9, discussed in paragraph 0049, which is formed from the data in fields 41 and 41', shows the table that provides a mapping from logical blocks to physical blocks.

23. **Claim 8** is taught by Conley as:

p. *The apparatus as claimed in claim 5, wherein the recovery operation recovers from an error by determining a latest accessed physical block for the logical block number among the detected physical blocks according to priorities set during the scanning process, as the valid block.* Conley paragraph 0050

shows that the most recently written page is determined by checking field 43, the timestamp.

q. *And rewriting flash memory state information written in other physical blocks of the detected physical blocks as deleted.* Paragraph 0062 shows that updating one or more blocks of data will result in one or more blocks storing the data to be superceded by the new data, and the blocks with superceded data are identified for erasure.

24. **Claim 9** is taught by Conley and Kim as:

r. *The apparatus as claimed in claim 5, wherein the recovery operation is performed during the initializing the flash memory.* Kim column 4 lines 22-25 shows that when a flash memory is initially used, a logical unit number to physical unit number table is provided. To generate such a table in a system using the timestamps of Conley, it would be necessary to determine which of the pages sharing the same logical block number and page offset is the most recent page.

25. **Claim 10** is taught by Kim as:

s. *The apparatus as claimed in claim 5, wherein the recovering from the error is performed during reclaiming the flash memory wherein the reclaiming comprises moving data written in a predetermined unit of the flash memory to a new unit.* Column 8 line 55 to column 9 line 4 teaches that in a reclaim operation,

valid blocks and related metadata are copied to a new unit. In order to determine which blocks are valid in a system using the timestamps of Conley, the timestamps of pages having the same logical block number and page offset must be compared.

26. **Claim 15** is taught by Conley as shown *supra* with respect to claim 11.

27. Although Conley teaches that blocks having the same logical block number can be distinguished by their timestamps, it does not disclose expressly performing a recovery operation.

28. With respect to claim 5, Kim teaches:

t. *The method as claimed in claim 11, further comprising a recovery operation comprising detecting, during a scanning process, physical blocks for the logical block number and of recovering from an error by determining a valid block for the logical block among the detected physical blocks.* Kim teaches at column 6 lines 29-36 that a recovery operation is required if two valid blocks having the same logical block number exist. In the system disclosed by Conley, paragraph 0050 shows that it can be determined which of multiple pages having the same logical block number and page offset is the correct page by comparing the timestamps of the blocks.

29. At the time of the invention it would have been obvious to one of ordinary skill in the art that a recovery operation is necessary in the event of an error during writing.

30. Conley and Kim are analogous art because they are from the same field of endeavor, the design of flash memory systems.

31. The motivation for doing so would have been to determine which block will be erased during a recovery operation (Kim, column 6 lines 30-36)

32. Therefore, it would have been obvious to combine Kim with Conley for the benefit of determining which pages are old and can be deleted to obtain the invention as specified in **claims 15 and 17**.

33. **Claim 17** is taught by Conley and Kim as:

u. *The method as claimed in claim 15, wherein the recovering comprises recovering from the error by determining a latest data written among data of a specific logical block number detected during reclaiming the flash memory and wherein the reclaiming comprises moving data written in a predetermined unit of the flash memory to a new unit.* Conley paragraph 0050 shows that the most recently written page is determined by checking field 43, the timestamp. Kim column 8 line 55 to column 9 line 4 teaches that in a reclaim operation, valid blocks and related metadata are copied to a new unit. In order to determine which blocks are valid in a system using the timestamps of Conley, the timestamps of pages having the same logical block number and page offset must be compared.

Response to Arguments

34. Applicant's arguments filed 11/27/2006 have been carefully and fully considered, and have been found partially persuasive.

35. **First point of Argument**

36. In the fourth paragraph of page 7 of the response filed 11/27/2006, Applicant argues with respect to the objection to the drawings that "*the dashed line indicates an optional ordering of operations. That is, operation (1) and (2) may either occur simultaneously or sequentially.*" Applicant's arguments, and the description of the invention at paragraphs [95]-[96], are sufficient to overcome the Examiner's objection to the drawings. Accordingly, the objection to the drawings has been withdrawn.

37. **Second point of Argument**

38. In the first paragraph beginning on page 8 of the response filed 11/27/2006, Applicant argues with respect to the rejection of claims 2, 3, 12, and 13 under 35 USC 112 first paragraph that "*the dashed line indicates an optional ordering of operations. That is, (1) and (2) may either occur simultaneously or sequentially. Further, page 15 paragraph [95] of the specification, for example, describes writing data in operation (1). Similarly, page 15, paragraph [96] of the specification, for example, describes writing flash memory state information (i.e., meta information) in operation (2).*" Applicant continues in the second paragraph beginning on page 8 that "*the cited portion, along with the drawings, disclose both the claimed features 'wherein the meta-information is written after the data of the logical block is written,' and, with regard to claims 3, and 13, 'wherein the data and meta-information of the logical block are simultaneously written.'*"

The Examiner respectfully notes that claims 2, 3, 12, and 13 were not rejected for failing to meet the written description requirement of 35 USC 112 first paragraph, but the enablement requirement of 35 USC 112 first paragraph. As known by one of ordinary skill in the art, flash memory differs from random access memory in that sections of memory must be written and erased in sections larger than the word level, among other differences. The discussion of figure 4 at paragraphs [50]-[52] show that the data and meta-information are stored in a single block of the flash memory. Paragraph [05] of the specification of the invention states "*in the flash memory, access is gained based on the block which written data is retrieved from or data is written in at once during read/write operations*". As data in a block can only be written at once during a write operation, and the data and meta-information are stored in a single block, there is no teaching of how the data and meta-information can be written separately. The Examiner agrees that the specification provides enablement for the limitation "*wherein the data and meta-information of the logical block are simultaneously written*" as recited in claims 3 and 13, and accordingly the rejection of claims 3 and 13 under 35 USC 112 first paragraph is withdrawn. However, the Examiner maintains the rejection of claims 2 and 12 under 35 USC 112 first paragraph, as the specification does not teach how "*the meta-information is written after the data of the logical block is written*" as required by claims 2 and 12.

39. **Third point of Argument**

40. In the third paragraph beginning on page 8 and continuing on page 9 of the response filed 11/27/2006, Applicant argues with respect to the rejection of claims 1 and 11 under 35 USC 112 second paragraph that "*The phrase 'if a previous write operation*

has not been performed for the logical block' is not limited to either situations noted by the Examiner. That is, 'if a previous write operation has not been performed' comprises any situation where a previous write operation has not been performed, not just the two scenarios set forth by the Examiner. Thus, applicant submits that the meaning of the claimed feature is definite in that it comprises any situation where a previous write operation has not been performed." This argument is found persuasive, and accordingly the rejection of claims 1 and 11 under 35 USC 112 second paragraph is withdrawn.

41. **Fourth point of Argument**

42. In the first paragraph beginning on page 9 of the response filed 11/27/2006, Applicant argues with respect to claims 6-10 and 12-17 that "*the claim amendments submitted herein obviate the informalities noted by the examiner*". The Examiner agrees, and accordingly the rejection of claims 6-10 and 12-17 under 35 USC 112 second paragraph is withdrawn.

43. **Fifth point of Argument**

44. In the second paragraph beginning on page 9 through the second paragraph beginning on page 10 of the response filed 11/27/2006, Applicant argues with respect to the rejection of claims 1, 3, 4, 11, 13, and 14 under 35 USC 102(b) that:

v. "*claim 1 requires, inter alia, that if the previous write operation for the logical block had completed, the flash controller writes the data and the meta-information in a new physical block without changing flash memory state information written in a previous physical block.*

w. *Conley, on the other hand, merely discloses a physical block having a logical block number and a timestamp. The time stamp used in Conley only indicates a time at which data was last written to the physical block. Moreover, a time stamp is different from state information since a time stamp indicates time, whereas state information indicates a status.*

x. *Conley fails to disclose anything related to state information, i.e., a status of the physical block itself. Indeed, Conley is silent on any such feature. Thus, Applicant respectfully submits that Conley fails to teach or suggest without changing flash memory state information written in a previous physical block, as claim 1 requires.*"

45. The Examiner respectfully disagrees for the following reasons. First, if Conley is interpreted to fail to disclose anything related to state information as argued by Applicant, although the Examiner disagrees with this interpretation, then Conley must teach writes without changing flash memory state information in a previous physical block. If Conley does not disclose anything related to state information, there is no state information to change in a previous physical block, and accordingly, writes in Conley are made without changing flash memory state information written in a previous physical block. Claims 1 and 11 do not recite writing state information, they merely recite writing meta-information, which is clearly taught by Conley figure 10 items 49 and 47.

46. However, The Examiner maintains that the time stamp of Conley is flash memory state information. Paragraph 0052 of Conley clearly states "*the controller, when called upon to read the data, easily distinguishes between the new and superceded pages'*

data by comparing the counts in the fields 43 and 43' of pages having the same LBA and page offset." Accordingly the time stamp of Conley, item 43 of figure 10, tells which page of multiple pages having the same LBA and offset are valid pages, and is therefore state information as recited in the claims.

47. **Sixth point of Argument**

48. In the second paragraph beginning on page 11 of the response filed 11/27/2006, Applicant argues with respect to the rejection of claims 6, 6, 8-10, 15, and 17 under 35 USC 103(a) that "*Kim fails to cure the deficiency of Conley as noted above regarding independent claims 1 and 11.*" The Examiner respectfully notes that Kim was not relied upon to teach the limitation "*the flash controller writes the data and the meta-information in a new physical block without changing flash memory state information written in a previous physical block corresponding to the logical block*". The Combination of Conley and Kim teaches claims 5, 6, 8-10, 15, and 17 as shown supra for the reasons noted with respect to Applicant's arguments with respect to Conley's teaching of said limitation.

Allowable Subject Matter

49. **Claims 7 and 16** are objected to as being dependent upon a rejected base claim, but may be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

50. **Claim 7** recites the limitation "*wherein the investigating the field of the block allocation table comprises writing a state value of "1" in the field of the block allocation*

table if the state value has been "0" and detecting that the logical block number has been searched for through the previous physical block during the scanning process, if the state value is "1"." This limitation in combination with the other recited limitations is not taught or suggested by the prior art of record.

51. **Claim 16** recites the limitation "*And writing a state value of "1" in the field of the block allocation table if the state value has been "0" and detecting that the logical block number has been searched for through the previous physical block during the scanning process, if the state value is "1".*" This limitation in combination with the other recited limitations is not taught or suggested by the prior art of record.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared I. Rutz whose telephone number is (571) 272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jared I Rutz
Examiner
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jir

Brian R. Peugh
Primary Examiner
2/7/07